International Journal on Emerging Technologies **4**(1): 32-38(2013)

ISSN No. (Print) : 0975-8364
ISSN No. (Online) : 2249-3255

A Power Gating Switch for Low Power 8 Bit CMOS Full Adder Circuit

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(Received 05 November, 2012, Accepted 21 February, 2013)

ABSTRACT: In most recent CMOS feature sizes (e.g., 90nm and 45nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. International technology roadmap for semiconductors (ITRS) reports that leakage power dissipation may come to dominate total power consumption. Leakage is mainly due to the scaling of CMOS. There are static and dynamic (switch mode) power losses occurs in CMOS circuit, in which static power is more important for sleep mode (no operation mode), leakage reduction improves the efficiency of the circuit, thereby saving a significant amount of energy. In static mode power consumption is the major drawback, As the biasing is remain in the internal circuit of the system there will be more sources of leakage in the internal circuits. In nano scale there are many sources (low threshold voltage, very thin gate oxide layer and band to band tunneling) which are responsible for the leakage of current. This paper propose an approach of using a power gating switch (PGS) to minimize the leakage of power because of fine scaling of CMOS. The purpose of employing PGSs in circuits is to reduce sleep power by strongly shut off the leakage paths during sleep modes, means there is no close loop between supply and ground. In this method at stand by condition leakage current will be minimized. Circuits are simulated in MICROWIND using 90nm and 45nm CMOS technology. The simulations will show leakage consumption can greatly be reduced by using the proposed power-gating switch compared with the MTCMOS power-gating Technique.

Keywords: MTCMOS, power gating switch, sleeps mode, standby mode, sub-threshold leakage, Clock Adiabatic Logic (CAL)

I. INTRODUCTION

There are several sources for the leakage currents: (i) sub threshold leakage current due to very low threshold voltage (*V*T), (ii) gate leakage current due to very thin gate oxide (*T*OX), (iii) Band-to-Band tunneling leakage current due to heavily doped halo. As a result of an exponential dependency on the reduction of the threshold voltage, sub-threshold leakage has the potential to become the dominant factor in sub-100nm generations [2, 3].

Most recent CMOS feature sizes (*e.g.,* 90nm and 45nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. International technology roadmap for semiconductors (ITRS) reports that leakage power dissipation may come to dominate total power consumption. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching or active and static power is consumed regardless of transistor switching.

Many previously proposed techniques, such as voltage and frequency scaling, on dynamic power reduction.

However, as the feature size shrinks, e.g., to 45 nm and 90nm, static power has become a great challenge for current and future technologies. This dissertation implements 4bit and 8 bit CMOS parallel adder circuit with an addition of clocked adiabatic logic with a power gating switch consisting of sleep transistor to minimize the leakage

Components of Power Dissipation are

$$P_{avg} = P_{switchin} + P_{short\text{-}circuit} + P_{leakage}$$

$$C_L \cdot V_{DD}^2 F_{clk} + I_{SC} \cdot V_{DD} + I_{Leakage} \cdot V_{DD}$$

There are many reasons for which leakage power losses occur
in CMOS circuit [3].

- Sub-threshold leakage (weak inversion current)
- Gate oxide leakage (Tunneling current)
- Channel punch through
- Drain induced barrier lowering

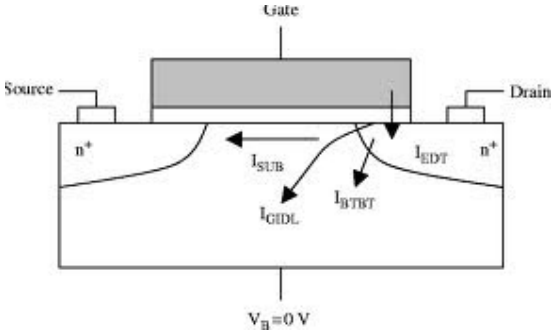

Fig. 1. Leakage power components in CMOS.

The sub-threshold leakage dissipation can be reduced significantly by controlling the threshold voltage of the devices. Various circuit techniques to control the sub-threshold leakage involve source biasing technique, input vector control technique, dual-threshold CMOS, power-gating techniques with multi-threshold CMOS (MTCMOS), and variable threshold CMOS (VTCMOS), However, these techniques.

Adiabatic logic is a promising low-power method to reduce the energy dissipation in digital circuits. Several adiabatic logic families and their applications have been reported and achieved considerable energy savings [5-7]. Similar to power-gating techniques of conventional CMOS circuits, power-gating schemes for adiabatic circuits have been also introduced to reduce energy loss during idle periods [8-9]. However, the previously reported power-gating adiabatic circuits are mostly investigated for reducing their dynamic energy dissipations during idle periods require significant circuit modification and performance overhead for leakage reduction [6-7].

This dissertation implements 4bit and 8 bit CMOS parallel full adder circuit with an addition of clocked adiabatic logic with a power gating switch consisting of sleep transistor to minimize the leakage

II. CLOCKED ADIABATIC LOGIC

The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. In this thesis work, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment.

The supply voltage in adiabatic circuits in addition to providing the power to the circuit behaves as the clock of the circuit and for this reason is called power clock. One of the main concerns in the adiabatic logic circuits is the power clock generation. In these circuits the supply voltage is desired to be a ramping voltage.

Although. it can be approximated by a sinusoidal voltage The improved CAL buffer is shown in Fig. 2(a) [7][9]. The logic evaluation circuit consists of the two NMOS transistors (N1, N2). CX is an auxiliary clock signal, and it enables the evaluation NMOS transistors (N1, N2) by turning on the NMOS transistors (N5, N6). The energy recovery circuit consists of the two cross-coupled PMOS transistors (P1, P2).power-clock (clk) charges the output (OUT or OUTb) in evaluation phase through P1 and P2. In recovery phase, the energy of the output nodes is recovered to clk through P1 and P2. The clamp transistors (N3 and N4) ensure stable operation by preventing from floating of the output nodes. The improved CAL circuits are supplied by a single-phase power clock, as shown in Fig. 2(a). The two phase non-overlap sinusoidal clocks (CX and CXb) are used for the auxiliary lines, as shown in Fig. 2(b). The two-phase sinusoidal clocks are generated with an auxiliary clock generator, as shown in Fig. 2(c) [7]. Its simulated waveforms are also shown in Fig. 2(d)

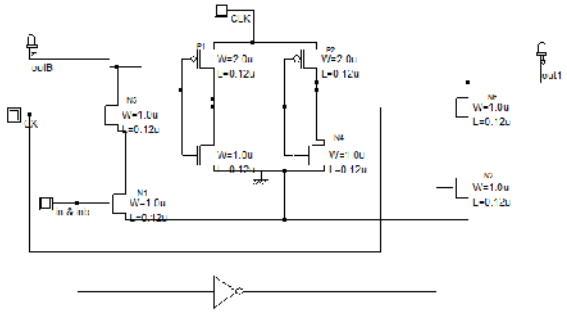

Fig. 2(a). CAL Buffer Circuit [7].

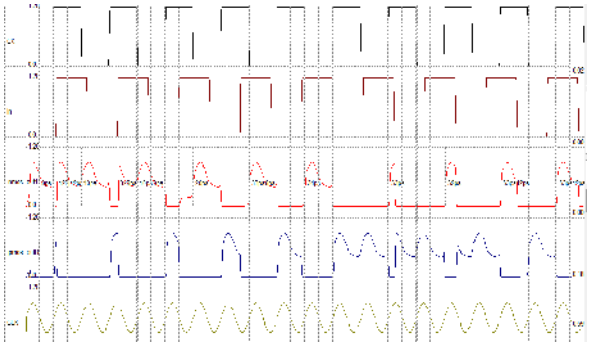

Fig. 2(b). Simulation Waveform.

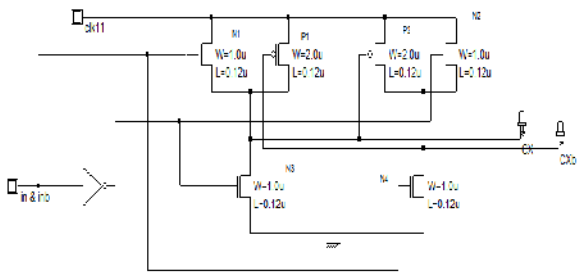

Fig. 2(c). Clock Generator [7].

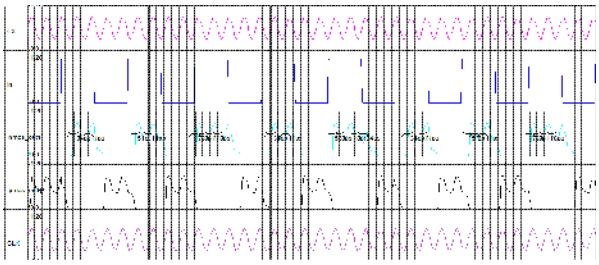

Fig. 2(d). Simulation Waveform.

III. TRANSMISSION GATE FOR SLEEP APPROACH

In the sleep approach, both (i) An additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) An additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Fig. 1 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

Similar to power-gating techniques of conventional CMOS circuits, adiabatic units can be also shut down by switching off their power-clocks to reduce energy loss during idle periods. The power-gating scheme for the improved CAL circuits is shown in Fig. 3. The transmission gate (TG) is used as the power-gating switch, which is inserted between the single phase power-clock (pc) and virtual power-clock (clk). It is used to disconnect the power-gated CAL logic blocks during idle periods In active mode, the power-gating control signal (Active) is high, thus clk follows the power-clock (pc). In sleep mode, Active is low, thus clk is set as low level, so that the power gated the power-gating adiabatic logic block.

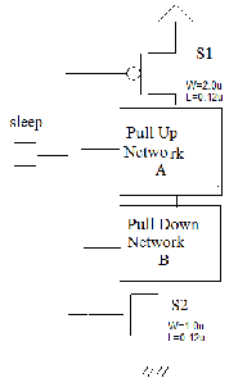

Fig. 3(a). Sleep Approach.

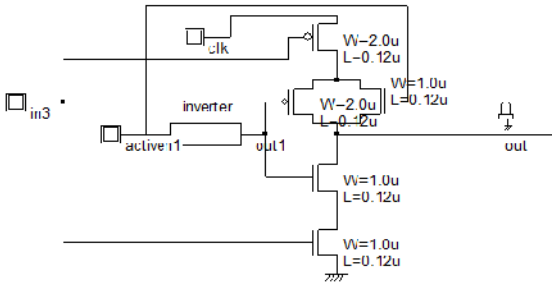

Fig. 3(b). Transmission gate using sleep input in 3.

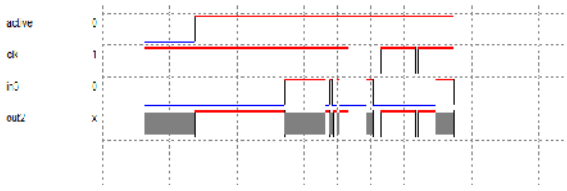

Fig. 3(c). Transmission Gate timing Waveform.

IV. MOTIVATION

Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important silent features like low power ,reliable performance and improvements in the processing technology. Large power dissipation requires larger heat sinks hence increased area. Cost of providing power has resulted in significant interest in power reduction of non portable devices sleep energy, which has become important in modern CMOS processes due to increasing contributions of sub threshold and gate.

Leakage current which affects total power consumption, and affects battery life. Therefore we have motivated to perform dissertation work in the accurate relative power measurement for effective reduction of leakage in sleep mode with less complexity and no overhead in the circuit.

V. PROPOSED METHODOLOGY

In this paper, we use an energy efficient power gating technique for adiabatic circuits.. Transmission gates with sleep transistors are used as the power-gating switches.

A 4 bit and 8-bit full adder based circuits is verified using the proposed power-gating technique. Energy consumption of the CAL based circuit is simulated as a function of frequency. The proposed approach demonstrates that the circuit reduces considerable amount of leakage power in the Nano scale CMOS integrated circuits and are simulated in 45nm, 90nm and 120nm technology using MICRO-WIND EDA tool.

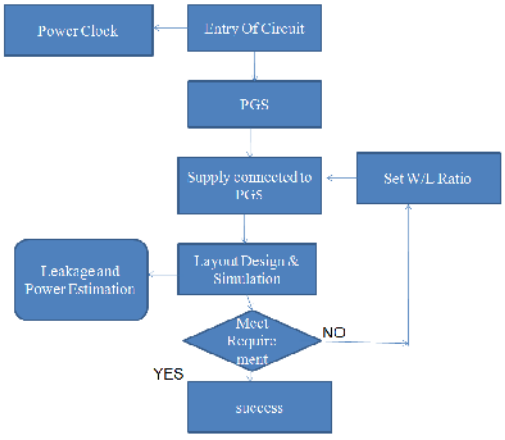

Fig. 4. Flow Chart.

In standby mode when sleep input is 1 power clock is disconnected from the functional block .devices s1 and s2 are high threshold devices therefore sub threshold conduction reduces at the cost of scaling of devices in 45nm and 90 nm. Therefore reduces leakage current and thus total power consumption reduces.

Desired power-clock frequency f, which is fed to the adiabatic block having frequency $f = \sqrt{1/2}\ LC_{eq}$ In the clock period A, the auxiliary clock CX enables the logic evaluation. For out = 0, compliment of function block are on, causing outb = 0 and M1 to be on, and thus allowing output out2 to closely follow the power clock waveform.

In the next clock period B, the auxiliary clock CX = 0 disables the logic evaluation. The previously stored logic state repeats at the outputs out1 and out2 regardless of the inputs, so that the stage that follows can perform logic evaluation. The logic evaluation is enabled in alternate logic stages by the auxiliary clock CX and its complement CX, at half the power clock rate [7][9].

The power-gating switches using a Transmission gate inserted between power-clocks clk and virtual power-clocks. They are used to disconnect the adiabatic logic block from the power-clocks during idle periods.

In order to reduce additional energy loss and obtain full swing operation of power gating switches should be energy efficient . The control signals ‘sleep’ feed the gates of S1 and S2 respectively. The sleep transistors S1 and S2 are high threshold voltage devices and the logic gate transistors are standard threshold voltage devices. This is to provide a well balanced trade-off between high speed and leakage loss. The CMOS circuit output can be drawn either between PUN and sleep circuit or between sleep circuit and PDN.

VI. IMPLEMENTATION

A 4 bit CMOS adder circuit is implemented in DSCH tool. Functional block is made up with adiabatic logic. A sinusoidal clock is supplied to the adiabatic logic. Power gating switch is used for providing supply voltage in active mode. And shut off the supply in standby mode.

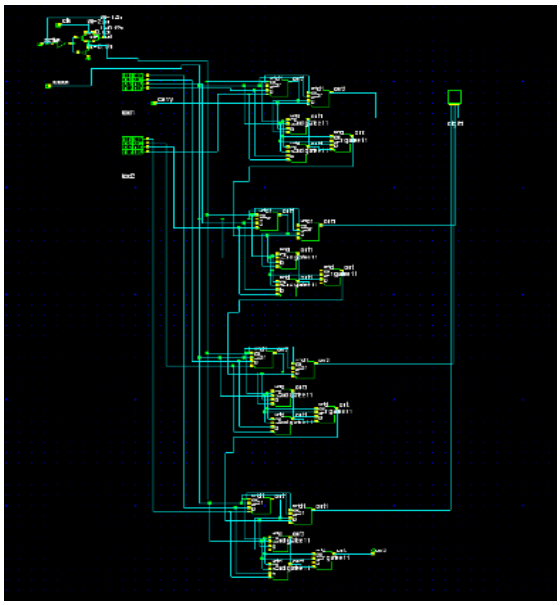

Fig. 5. Implementation of 4-Bit full adder in MICROWIND.

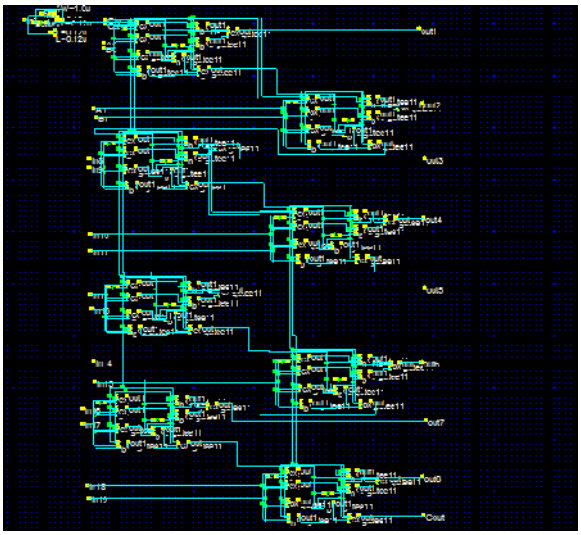

Fig. 6. Implementation of 8 Bit fulladder in MICROWIND.

VII. RESULTS

Compared with MTCMOS, proposed scheme can well reduce the total power consumption .At 90 nm CMOS technology, the 8 bit improved CAL adder with proposed scheme attains energy savings of 26.9% to 27.6% with the frequency changing from 1000 to 3000 MHz .

At 45 nm CMOS technology, the 8 bit improved CAL adder with proposed scheme attains energy savings of 22.6.9% to 28.0% with the frequency changing from 1000 to 3000 MHz.

Table 1, 2, 3 and 4 shows the leakage power consumption reduction and the total power consumption reduction of 8 bit and 5 bit improved CAL adders with proposed scheme compared with the MTCMOS in 45nm CMOS technology and 90 nm CMOS technology ,respectively. As we can see that Table 1 and 2 with the scaling of reduction of processes ,the leakage power loss of CAL circuits can be reduced more effectively by using power gating switch.

Power consumption for 8 bit adder

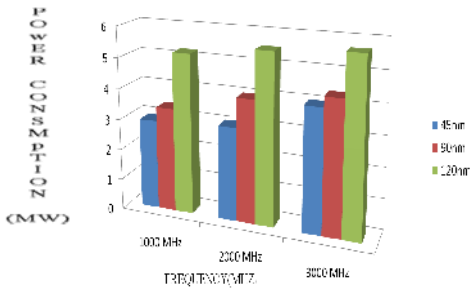

Table 1: Power Loss Reduction of 8 Bit CAL Full Adder Using Power Gaitng Switch at 45nm Process Compared with Base Case.

%Power Reduction (45nm)	**Frequency (MHz)**		
	1000	2000	3000
STATIC POWER	36.3	34.2	31.7
TOTAL POWER CONSUMPTION	28.2	27.1	22.0

Table 2: Power Loss Reduction of 8 Bit CAL Full Adder Using Power Gaitng Switch at 90nm Process Compared with Base Case.

%Power Reduction (90nm)	**Frequency(MHz)**		
	1000	2000	3000
STATIC POWER	31.6	28.2	23.6
TOTAL POWER CONSUMPTION	21.3	18.5	15.2

Table 3: Power Loss Reduction of 4 Bit CAL Full Adder Using Power Gaitng Switch at 45nm Process Compared with Base Case.

%Power Reduction (45nm)	**Frequency(MHz)**		
	1000	2000	3000
STATIC POWER	45.6	41.3	37
TOTAL POWER CONSUMPTION	27.6	27	26.8

Table 4: Power Loss Reduction of 4 Bit CAL Full Adder Using Power Gaitng Switch at 45nm Process Compared with Base Case.

%Power Reduction (120nm)	**Frequency(MHz)**		
	1000	2000	3000
STATIC POWER	37.8	35.6	35.4
TOTAL POWER CONSUMPTION	19.1	17.3	13.2

Simulation Result

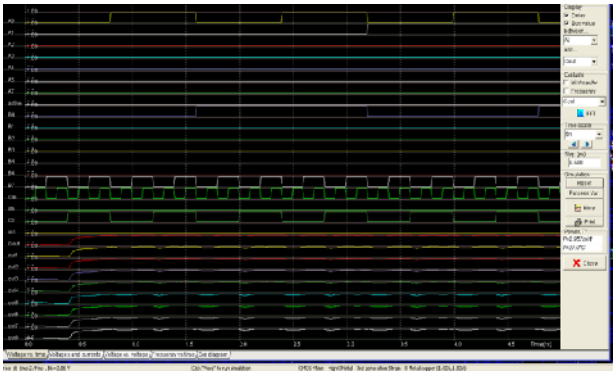

Fig. 7(A). Simulation Waveform of 8 Bit CAL Full Adder at 45nm Process.

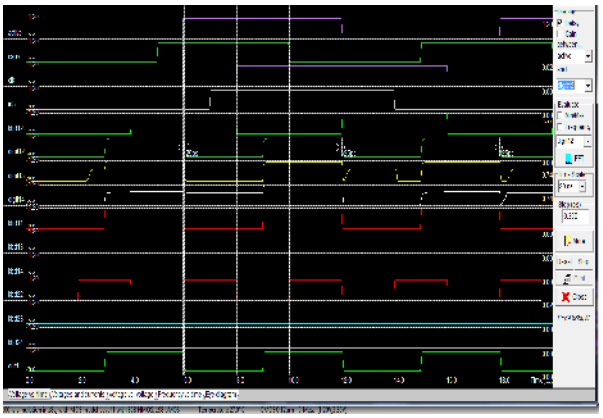

Fig.7(B). Simulation Waveform of 4 Bit CAL Full Adder.

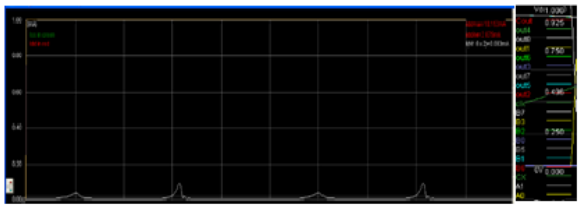

Fig. 7(c). Leakage Current in 4 Bit CAL Full adder.

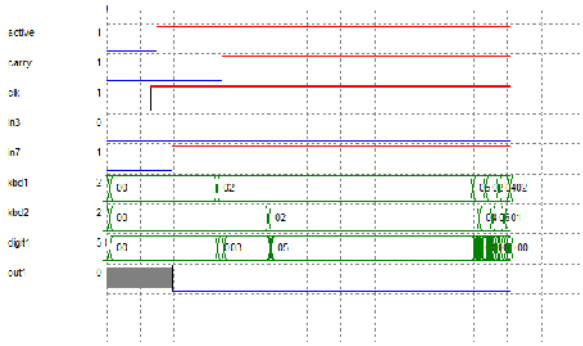

Fig. 7(D). Timing Waveform of 4 Bit CAL Full Adder.

VIII. CONCLUSION

This paper presents designing and simulation of 8 Bit and four Bit low power CMOS full adder circuit. Results shows that by introducing a power gating switch, leakage power loss and total power loss of 4 bit and 8 bit adder can be reduced by 20-30 by percent.

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